A 4.9mW 270MHz CMOS Frequency Synthesizer/FSK Modulator

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Abstract — **A 270MHz frequency synthesizer/FSK modulator for low-rate WPAN is implemented. It consumes only 4.9mW adopting current re-using technique, self-DC biasing scheme, and appropriate divider architecture. The 3rd-order feedback type DSM and the high performance charge pump are designed for wide loop bandwidth, which enables to design a low power and low noise frequency synthesizer. The implemented prototype offers 500kHz-loop bandwidth and −104dBc/Hz in-band noise. It also plays a role as a FSK modulator which shows only 1.1 dB degradation at 10^{-3} symbol BER compared with the ideal FSK-modulator.**

I. Introduction

In mobile communication systems, low power capability is important because it brings the long battery life and good autonomy. Especially, for Low-Rate Wireless Personal Area Network (LR-WPAN) system like distributed wireless micro-sensor, RF ID card, and toys application, power consumption is the essential property.

Fig. 1 shows the block diagram of PLL direct modulator architecture. While the conventional I/Q modulator requires two DACs, LPFs, an up-mixer, and a frequency synthesizer, this architecture needs only a frequency synthesizer. This simple architecture can lead to extremely low power consumption, and is suitable for the transmitter of LR-WPAN system.

In PLL direct modulator, wide loop bandwidth is highly desired because of two reasons. Firstly, high energy-efficiency is required for low power applications, which is controlled by duty rate between active mode time and sleep mode time. Especially, in LR-WPAN applications, the startup time is comparable with active mode time. Therefore, fast startup time of a frequency synthesizer is very important, which is dominated by loop bandwidth [1]. Secondly, the loop bandwidth limits the modulation data rate and as the higher data rate, the wider loop bandwidth is required [2].

Several papers have made an effort for the high data rate transmission with the narrow loop bandwidth such as pre-amplifying scheme [2] or two-port modulation [3]. But these schemes require the exact matching, which means hard trimming. Furthermore, for diminishing the trimming effort, the automatic calibration scheme was proposed [4]. However, this approach requires additional power consu-

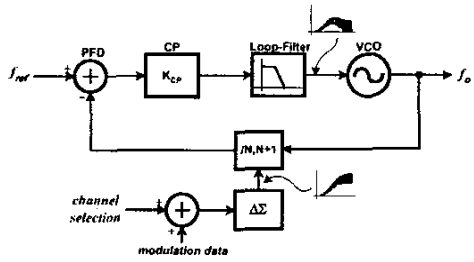

Fig. 1. PLL direct modulator architecture

mption due to its compensation and calibration circuitry. Therefore, for increasing data rate, the bandwidth widening approach is more suitable for energy efficient LR-WPAN systems because existing compensation techniques in previous works is hard to implement and consumes more power. The wider loop bandwidth means faster startup as well as higher data rate.

For wide loop bandwidth, high reference frequency is desired. Since Delta-Sigma Modulator (DSM) quantization noise appears at the half of the reference frequency, the noise from higher reference clock can be effectively removed although a loop filter has wide bandwidth. When using high reference frequency, charge pump should be carefully designed because the rising and falling time can be ignored no longer. Furthermore, mismatches affect in-band noise characteristic and reference spurious tone power.

The target output frequency band for this prototype is 267MHz~273MHz and I/Q frequency synthesis is required for direct conversion receiver. The chip rate is assumed to be 231kcps (21kbps × 11barker-sequence), and modula-tion index is 2.5.

II. System Implementation

A. Architecture

Fig. 2 shows the functional block diagram of the 4th-order PLL prototype. DSM is implemented externally for the flexible measurement of this prototype. To ensure the

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excellent I/Q signal generation and avoid oscillator-pulling effect by antenna-buffer, the VCO oscillation frequency is

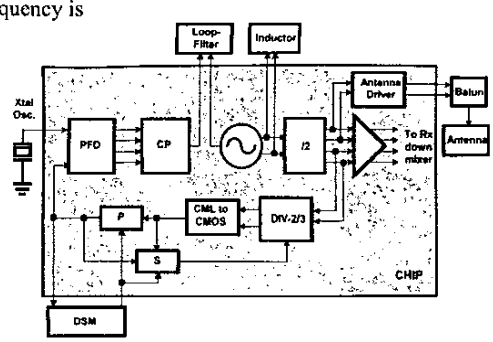

Fig. 2. Functional block diagram of the prototype

set to 540MHz, twice of RF carrier frequency, and a fixed divide-by-2 circuit is used. Replica of divide-by-2/3 block and off-condition input capacitance of antenna buffer is also inserted to make the symmetry load of divide-by-2 for the good I/Q matching of the LO signal to the receiver.

Frequency divider is composed of the combination of current mode logic (CML) and CMOS static logic. In high frequency blocks, such as a fixed divide-by-2 and a divide-by-2/3 block, CML scheme is adopted, while the other low frequency blocks are implemented using CMOS static logic, which shows good power efficiency. All CML blocks are implemented with resistive load for wide bandwidth.

3rd-order feedback type DSM with 1-bit quantized output was designed, which has better noise shape than that of MASH architecture DSM [5]. 41MHz reference frequency was chosen for the sufficient suppression of the DSM noise. The loop simulation is accomplished using Matlab.

B. Synthesizer Building Blocks

In lower than 540MHz frequency, DC blocking capacitor cannot be used freely due to large area. For DC-level converter, it is hard to be adopted because of its additional power consumption. Consequently, careful design of self DC-biasing is needed in the interface of each block for low power consumption.

Fig. 3 shows the VCO circuit schematic that uses PMOS cross-coupled pair as well as the NMOS devices for symmetry. Using the PMOS current source, VCO is strong to supply noise. The lower NMOS diode corresponding to the upper PMOS current source can help to adjust the output DC bias automatically.

Fig. 4 shows D-Flip-flop with NAND, the core circuit of divide-by-2/3 block. The NAND circuit and the D-Flip-flop circuit are merged to reuse the current drawn.

The charge pump is shown in Fig 5. As mentioned in previous section, this frequency synthesizer has wide loop

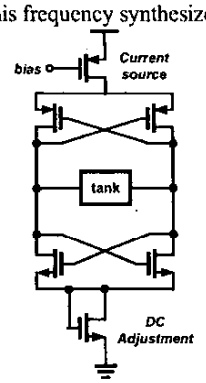

Fig. 3. Stacked CMOS cross-coupled negative-gm VCO

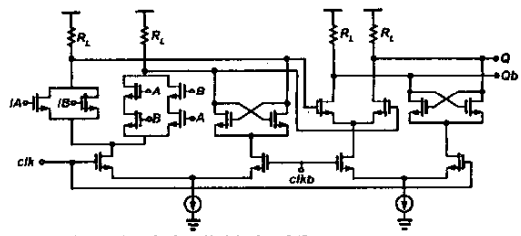

Fig. 4. Core circuit for divide-by-2/3

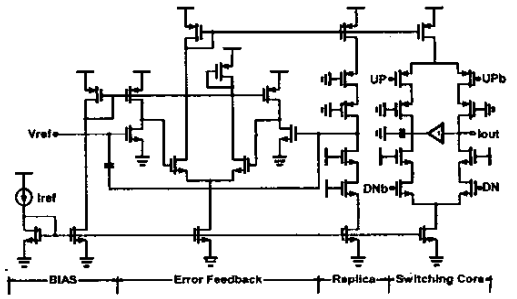

Fig. 5. Charge pump

bandwidth for low power consumption, which means it is more sensitive to the current mismatch in charge pump. For this reason, it is required to minimize the mismatch in charge pump. To prevent up/down DC current mismatch, replica and error feedback circuit are implemented. Replica circuit reproduces up/down DC current mismatch of the switching core, and then it is negatively fed back to decrease the mismatch.

When the current is switched by the input, unity gain OP-amp helps to minimize charge re-distribution. The dummy complementary transistors are inserted in parallel to the input transistor of switching core to balance the differential loads of PFD.

III. Experimental Results

The 270MHz Frequency Synthesizer/FSK modulator was fabricated in TSMC 0.18um CMOS process with 1135um × 726um of die area as shown in Fig. 6. It is packaged in a TQFP package and the external 27nH inductor is used for VCO. DSM was implemented using Xilinx FPGA. The supply voltage is 1.8V.

A. Frequency Synthesizer

Output phase noise in open loop condition is –103dBc/Hz at 100kHz offset, while –120dBc/Hz at 700kHz offset.

Using the least significant bit of DSM input, the accurate output frequency is obtained with the resolution of 78.2Hz. The measured phase noise in closed loop is shown in Fig 7. The in-band phase noise is as low as –104dBc/Hz at 10kHz offset and the DSM noise is –100dBc/Hz at 2MHz offset. The –58dBc/Hz reference spurious tone is mainly caused by a large DSM driving buffer to drive external DSM with large FPGA digital noise, which can be eliminated by single chip integration.

The settling time is less than only 7usec when output frequency moves from the lowest to the highest of the application frequency band. The fast turn-on time leads to the low power consumption of the entire system.

B. FSK Modulator

Chip '101010...' with 231kcps is assumed as the worst case of input. The modulated output spectrum in this case is shown in Fig 8.

Fig. 9 shows the simulated BER performance when the receiver is assumed to adopt direct conversion architecture and segmented semi-coherent demodulator, and the transmitter is assumed to use this frequency synthesizer. It shows only 1.1 dB degradation at 10^{-3} symbol BER compared with the ideal FSK-modulator.

C. Overall Results

The measured power consumption of building blocks and the summary of the measured performance are shown in Table I. The measured power consumption of a frequency synthesizer is 4.9mW except LO buffer and antenna driver. When the prototype is in RX mode (LO buffer: on, antenna driver: off), it consumes 5.8mW, while 8.5mW in TX mode (LO buffer: off, antenna driver: on). The external DSM can be integrated into a single chip frequency synthesizer/modulator with the estimated power consumption of less than 0.5mW at 41MHz operating frequency. Table II shows the performance comparison with other works. Although VCO frequency is considered, this work shows excellent power and noise performance.

TABLE I
POWER CONSUMPTION OF BUILDING BLOCKS & SUMMARY OF THE MEASURED PERFORMANCE

VCO	259uA
DIV by 2 + Divider +PFD	1531uA
Charge Pump	930uA
LO Buffer	505uA
Ant Drv. (-10dBm output power)	2000uA
Total (w/o LO Buff. & Ant Drv.)*	2720uA (4.9mW)
Total (RX)*	3225uA (5.8mW)
Total (TX)*	4720uA (8.5mW)

Supply Vtg.	1.8V
Supply Current*	2720uA
Output Freq.	270MHz (540MHz /2)
Ref. Freq.	41MHz
Loop BW	500kHz
Min. Freq. Resolution	78.2Hz
PN@10kHz offset	-104dBc/Hz
Ref. Spur.	-58 dBc/Hz

*: except DSM

IV. Conclusion

A 270MHz frequency synthesizer/FSK modulator with 500kHz loop bandwidth is implemented. It consumes only 4.9mW adopting current re-using technique, self-DC biasing scheme, and appropriate divider architecture. The 3rd-order feedback type DSM and the high performance charge pump help to achieve wide loop bandwidth, which

TABLE II
PERFORMANCE COMPARISON WITH OTHER WORKS

Ref.	Tech.	Arch.	f_{vco}	f_{ref}	f_{BW}	f_{ref} / f_{BW}	In-band noise @10KHz offset	Power
Rhee et al., 2000[5]	0.5um CMOS	3rd-order 3-bit	900MHz	8MHz	40kHz	200	-92dBc/Hz	29mW (w/o VCO)
Hegazi et al., 2002[6]	0.35um CMOS	3rd-order MASH	900MHz	13MHz	90kHz	144	-80dBc/Hz	17.4mW
Rhee et al., 2002[7]	0.35um BiCMOS	3rd-order 3-bit	2.5GHz	8MHz	35kHz	229	-82dBc/Hz	16mW (w/o VCO)
This work	0.18um CMOS	3rd-order 1-bit	540MHz	41MHz	500kHz	82	-104dBc/Hz	4.9mW (w/o DSM)

enables to design a low power, low noise frequency synthesizer.

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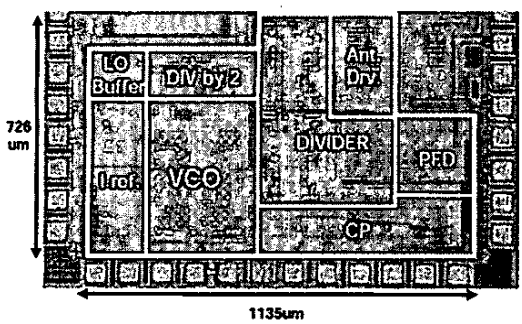

Fig. 6. Die micro-photograph

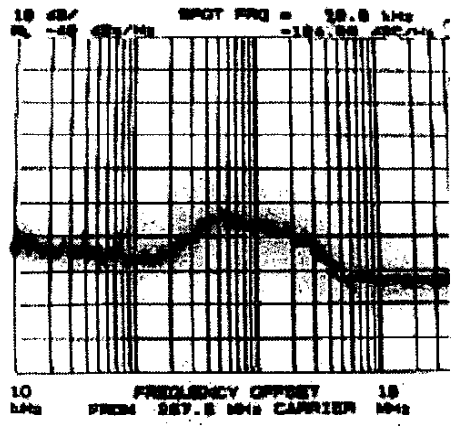

Fig. 7. Closed loop output phase noise

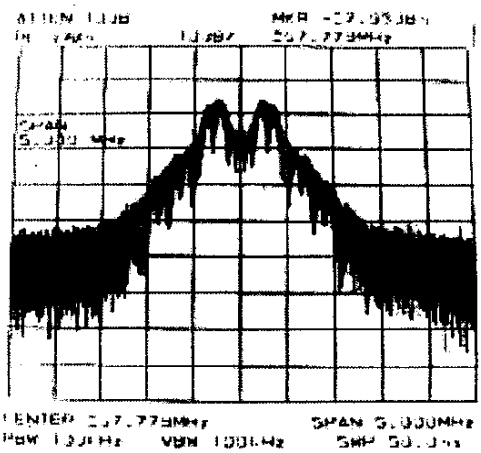

Fig. 8. Modulated output spectrum for 231kcps chip rate worst case

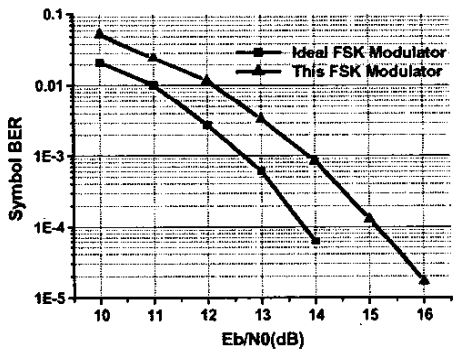

Fig. 9. Symbol bit error rate